CC/AF/2814
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Docket No.: PEK-In1512

MAIL STOP: APPEAL BRIEF-PATENTS

By: _____ Date: May 24, 2004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

Applic. No.	:	10/045,278 Confirmation No.: 4446
Inventor	:	Oliver Gehring et al.
Filed	:	January 14, 2002
Title	:	Method for Fabricating Embedded Nonvolatile Semiconductor Memory Cells
TC/A.U.	:	2814
Examiner	:	Marcos D. Pizarro Crespo
Customer No.	**:**	**24131**

Hon. Commissioner for Patents
Alexandria, VA 22313-1450

BRIEF ON APPEAL

S i r :

This is an appeal from the final rejection in the Office action dated January 28, 2004, finally rejecting claims 1-10.

Appellants submit this *Brief on Appeal* in triplicate, including payment in the amount of $330.00 to cover the fee for filing the *Brief on Appeal*.

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Real Party in Interest:

This application is assigned to Infineon Technologies AG of München, Germany. The assignment will be submitted for recordation upon the termination of this appeal.

Related Appeals and Interferences:

No related appeals or interference proceedings are currently pending which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

Status of Claims:

Claims 1-10 are rejected and are under appeal. No claims were cancelled.

Status of Amendments:

No claims were amended after the final Office action. *A Notice of Appeal* was filed on April 2, 2004.

Summary of the Invention:

As stated in the first paragraph on page 1 of the specification of the instant application, the invention relates to a method for fabricating embedded nonvolatile semiconductor memory cells and, in particular, to a method for fabricating nonvolatile memory cells in a semiconductor

circuit with at least a high-voltage region and a logic region.

Applicants explained on page 7 of the specification, line 21, that, referring now to the figures of the drawing in detail and first, particularly, to Figs. 1A and 1B thereof, there is shown a respective plan view and a sectional view of a semiconductor circuit with a high-voltage region HVB, a nonvolatile memory region NSB and a logic region LB. In accordance with the invention, nonvolatile semiconductor memory cells are accordingly intended to be formed in the nonvolatile memory region NSB, the intention being simultaneously to form corresponding switching elements of high-voltage transistors and logic transistors in the further high-voltage and logic regions HVB and LB. Since, as has already been discussed in the introduction, the switching elements have to satisfy requirements that differ and often even conflict, the description below describes a particularly advantageous processing in particular for the purpose of realizing so-called embedded nonvolatile semiconductor memory cells. In this case, the invention essentially relates to the formation of first layers on a substrate, for which reason the processing for forming active regions and different doped wells in the substrate and also the formation of "upper" layer sequences are not discussed in any further detail below.

Appellants outlined on page 8 of the specification, line 17, that, in accordance with Fig. 1B, after the formation of active regions for example by shallow trench isolation (STI), in the nonvolatile memory region NSB, a first insulating layer 2 is formed on a substrate 1, which constitutes a silicon semiconductor substrate 1 for example. The first insulating layer 2 may be formed by a deposition method, for example, and preferably is formed as a silicon oxide layer having a thickness of 20 to 25 nm. As an alternative, however, it is also possible for thermal formation to take place.

It is stated on page 9 of the specification, line 1, that, in accordance with Fig. 2A and Fig. 2B, in a subsequent fabrication step, the first insulating layer 2 is locally removed in the nonvolatile memory region NSB. The patterning is carried out for example using a non-illustrated lithographic mask, wet-chemical or dry-chemical processes being used to remove the first insulting layer 2 with subsequent resist stripping. The formation of possibly required wells and other doping regions in the respective regions of the semiconductor circuit is explicitly dispensed with at this point since this involves steps that are not essential to the invention.

It is further stated on page 9 of the specification, line 13, that, in accordance with Figs. 3A and 3B, a second insulating layer 3 is formed over the whole area. By way of example, the second insulating layer 3 is formed thermally in a furnace process or by a rapid thermal process (RTP), a tunnel oxide layer 3 having a thickness of approximately 7 to 10 nm preferably being formed as a result. In the nonvolatile memory region NSB, the tunnel oxide layer 3 is used as a tunnel layer 3 for the respective nonvolatile semiconductor memory cells, whereas, particularly in the high-voltage region HVB, together with the first insulating layer 2, it forms a high-voltage oxide layer 4 approximately having a thickness of 25 to 35 nm. In this case, the reduced thickness essentially results from the reduced oxide growth on the first insulating layer 2.

Appellants outlined on page 10 of the specification, line 2, that, in a further fabrication step in accordance with Figs. 4A and 4B, there then takes place whole-area formation and patterning of a charge-storing layer 5 with a third insulating layer 6, in which case, in accordance with a first exemplary embodiment illustrated in Fig. 4B, the charge-storing layer 5 is deposited over the whole area for example as a highly doped (in-situ) polysilicon layer and is then patterned in the vertical direction for example above the trench isolation STI.

In a subsequent step, the third insulating layer 6 is formed over the whole area, which layer may contain for example an oxide-nitride-oxide (ONO) layer sequence. Particularly in the nonvolatile memory region NSB, the third insulating layer 6 serves as a coupling layer 6 and is also referred to as a coupling oxide layer 6. Particularly on account of the exclusive patterning of the charge-storing layer 5 with subsequent formation of the third insulating layer 6, the sidewalls of the charge-storing layers 5, formed in a strip-type manner, can be insulated particularly well, which has a favorable effect on the charge retention capability of memory cells.

It is further outlined on page 10 of the specification, line 23, that, as an alternative to the conductive charge-storing layer 5 described above, a nonconductive charge-storing layer can also be used in the same way, as a result of which the charge retention properties of nonvolatile semiconductor memory cells can be improved further.

Appellants explained on page 11 of the specification, line 4, that, in the same way, instead of the oxide-nitride-oxide (ONO) layer sequence 6, for the third insulating layer 6, it is possible to use a different dielectric as a coupling layer, in particular layers having a high relative permittivity

promoting a reduction of read/write voltages in the nonvolatile memory region NSB. In this case, programming is affected preferably via Fowler-Nordheim tunneling or injection of hot charge carriers through the second insulating layer 3 or tunnel oxide layer.

Appellants also explained on page 11 of the specification, line 14, that, in a further fabrication step in accordance with Figs. 5A and 5B, the first to third insulating layers 2, 3 and 6 and also the charge-storing layer 5 are then removed locally in the logic region LB. In this case, it is preferably to carry out dry-chemical etching of the third insulating layer 6 and of the charge-storing layer 5, which, for example, may also be effected jointly or simultaneously with the patterning of the charge-storing layer 5 and/or of the third insulating layer 6 in the nonvolatile memory part NSB in accordance with Figs. 4A and 4B. As an alternative, however, wet-chemical etching of the logic region LB can also be carried out.

It is mentioned on page 12 of the specification, line 1, that, afterward, for example using a wet-chemical etching operation, the high-voltage oxide layer 4 containing the first and second insulating layers 2, 3 is removed in the logic region, buffered or dilute hydrofluoric acid (HF) preferably being

used. In this way, the previously applied layers are removed down to the surface of the substrate 1 in a large-area manner and relatively gently, a very good substrate surface without dislocations and impurity atoms being obtained.

It is also mentioned on page 12 of the specification, line 10, that, on the basis of this very good substrate surface with a very small number of defects, a fourth insulating layer 7 can be formed over the whole area in a subsequent process step, which insulating layer, particularly in the logic region, fully satisfies the high demands - made with regard to breakdown strength - with regard to reliability. By way of example, the fourth insulating layer 7 is formed thermally as a gate oxide layer (SiO_2) by a furnace process or RTP method. However, it can also be deposited from the vapor phase.

Appellants stated in the last paragraph on page 12 of the specification, line 20, that, finally, a conductive control layer 8 is formed in a subsequent fabrication step, an electrically conductive polysilicon layer, for example, being deposited and patterned by a TEOS hard mask, for example. As an alternative, however, undoped polysilicon can also be deposited and subsequently implanted or a metallic layer can be deposited as the control layer 8. Preferably, during the patterning of the control layer 8, in the nonvolatile memory

region NSB, the coupling layer or the third insulating layer 6 as well as the charge-storing layer 5 are also patterned simultaneously, thereby producing island-type charge-storing layer regions or nonvolatile semiconductor memory cells. In the same way, corresponding switching transistors can also be formed in the high-voltage HVB.

Appellants explained on page 13 of the specification, line 9, that Fig. 5C shows a simplified sectional view in accordance with a section VC-VC from Fig. 5A in the high-voltage region HVB, a high-voltage transistor HVT now containing a stack formed by the control layer 8, the fourth and third insulating layers 7 and 6, the charge-storing layer 5 and the high-voltage oxide layer 4. The charge-storing layer 5 can preferably be removed in a previous step or be short-circuited with the control layer 8. Source regions S and drain regions D can be formed at this point in time, for example, in a self-aligning manner in the substrate 1. However, they can also be formed at a later or earlier point in time by different methods.

It is outlined in the last paragraph on page 13 of the specification, line 21, that Fig. 5D shows a sectional view in accordance with a section VD-VD shown in Fig. 5A, a nonvolatile memory transistor NST again containing the control

layer 8, the third and fourth insulating layers 6 and 7, the charge-storing layer 5 and the tunnel oxide layer or second insulating layer 3. Corresponding source regions S and drain regions D can again be formed in a self-aligning manner by ion implantation, for example, in the substrate 1.

As set forth on page 14 of the specification, line 4, Fig. 5E shows a simplified sectional view along a section VE-VE in accordance with Fig. 5A in the logic region LB, a switching transistor ST having only the control layer 8 and an extremely high-quality gate oxide layer as the fourth insulating layer 7.

Appellants also stated on page 14 of the specification, line 10, that, accordingly, the fabrication method described above can be used to fabricate in particular embedded nonvolatile semiconductor memory cells or transistors NST in a nonvolatile memory region NSB in a simple and cost-effective manner, at the same time in particular the electrical properties of switching transistors ST in the corresponding logic regions LB is not impaired. The insulating layers which are required for the respective characteristic properties and lie directly on the substrate 1 can thus be fabricated in a simple and cost-effective manner with high quality in an identical method.

Appellants outlined in the last paragraph on page 14 of the specification, line 21, that the invention has been described above using silicon semiconductor substrates. However, it is not restricted thereto and includes alternative substrate materials in the same way. In the same way, the invention is not restricted to the silicon dioxide, polysilicon and ONO layers described, but rather includes alternative materials in the same way.

References Cited:

U.S. Patent No. 6,194,036 B1 (Babayan et al.), dated February 27, 2001;

U.S. Patent No. 6,261,964 B1 (Wu et al.), dated July 17, 2001;

U.S. Patent No. 6,316,293 B1 (Fang), dated November 13, 2001;

Ghandhi: "VLSI Fabrication Principles - Silicon and Gallium Arsenide", A Wiley-Interscience Publication.

Issues

1. Whether or not claims 1, 3-6 and 9 are anticipated by Fang U.S. Patent No. 6,316,293 under 35 U.S.C. §102(e).

2. Whether or not claim 2 is obvious over Fang in view of Babayan U.S. Patent No. 6,194,036 under 35 U.S.C. §103.

3. Whether or not claims 7 and 8 are obvious over Fang in view of Ghandhi publishing an article entitled "VLSI Fabrication Principles Silicon and Gallium Arsenide" under 35 U.S.C. §103.

4. Whether or not claim 10 is obvious over Fang in view of Wu U.S. Patent No. 6,261,964 under 35 U.S.C. §103.

Grouping of Claims:

Claim 1 is independent. Claims 2-10 depend ultimately on claim 1. The patentability of only claim 1 is argued. Therefore, claims 2-10 stand or fall with claim 1.

Arguments:

The second through fourth paragraphs of claim 1 of the instant application recite:

> providing a substrate divided into a high-voltage region, a memory region and a logic region;
>
> forming a first insulating layer on the substrate in the high-voltage region, the memory region and the logic region; and
>
> removing the first insulating layer in the memory region.

The Examiner is believed to be stating that these features are shown in Fang by:

> the substrate 104 being provided and divided into three regions including a low voltage peripheral region 116 (see Fig. 5h), a core memory cell region 105 (Fig. 5a and equivalent to the memory area of the instant application), and a high voltage peripheral region 118 (Fig. 5h);
>
> an oxide layer (e.g. insulation layer) 108 disposed on all three regions 116, 105, 108; and
>
> the insulation layer 108 is removed in the area of the core region 105 (the memory region) (see Fig. 5c).

We agree with the Examiner that Fang reads on paragraphs 2-4 of the claim 1 of the instant application.

However, the fifth paragraph of claim 1 of the instant application reads:

> forming a second insulating layer in the high-voltage region, the memory region and the logic region; (emphasis added).

The Examiner states that this feature is shown in Fang by:

> forming a second insulating layer 110 (e.g. tunnel oxide layer 119) in the high-voltage region, the memory region and the logic region 116, 105, 118.

We respectfully disagree. The tunnel oxide layer 119 does not cover regions 116 or 118 (e.g. the equivalent regions to the high voltage region and the logic region) as shown in Figs. 5d and 5h.

As is also explained on page 9, lines 18-24 of the instant application, the tunnel oxide layer 3 (second insulating layer claim 1), together with the first insulating layer 2, forms a high-voltage oxide layer 4. The high-voltage oxide layer 4 is an important element of the present invention, especially in the high-voltage region.

Clearly, Fang does not disclose forming a second insulating layer over the high-voltage region, a nonvolatile memory region, and a logic region as recited in claim 1 of the instant application.

As is clearly described in column 6, lines 29-36 of Fang, the tunnel oxide layer 119 is only grown in a region 114 of the core region 105.

Paragraphs 6-8 of claim 1 of the instant application recite:

> forming a charge storing layer in the high-voltage region, the memory region and the logic region;
>
> patterning the charge-storing layer in the memory region; and
>
> forming a third insulating layer in the high-voltage region, the memory region and the logic region.

The Examiner is believed to be stating that these features are shown in Fang by:

> forming a charge storing layer 122 in layers 116, 105 and 118 (Fig. 5d);
>
> patterning the charge storing layer in the memory region 105 (Fig. 5e, 5f); and
>
> forming a third insulating layer 130 in the regions 116, 105, and 118 (column 7, lines 4-8).

Assuming the third insulating layer is applied area wide (e.g. not overly clear in Fang) and than patterned, applicant agrees with the Examiner.

However, the ninth paragraph of claim 1 of the instant application reads:

> removing the first to third insulating layers and also the charge-storing layer in the logic region (emphasis added).

The Examiner is believed to be stating that this feature is taught in Fang by:

> removing the first to third insulating layers and also the charge-storing layer from the logic region being 116 or 118 (see Fig. 5h).

Applicant respectfully disagrees. This cannot occur as the regions 116 and 118 are only covered by the first 108 and

arguably the third insulation layer 130. Simply put there is no second insulation layer 119 over either of these areas.

The tenth paragraph of claim 1 of the instant application reads:

> forming a fourth insulating layer in the high-voltage region, the memory region and the logic region.

The Examiner is believed to be stating that this feature is taught in Fang by:

> forming a fourth insulation layer in the high voltage region, the memory region and the logic region 116, 106, 118 (see column 7, lines 10-34).

Applicant respectfully disagrees. Column 7, lines 10-34 of Fang clearly teach that after the third insulation layer 130 is applied, an oxidation step occurs resulting in an intermediate oxide layer 137 which is etched away from region 116 but not from region 105 because an oxide does not grow appreciably on an ONO layer 130 and therefore no intermediate layer 137 is formed in the core region 105.

It is further noted that the oxide layers 140 or 142 do not form in the core region 105 as noted in column 7, lines 26-36 of Fang.

As is well known, an anticipation rejection under 35 U.S.C. §102(e) must teach all of the steps or features recited in the claim language. As at least three of the steps or features of the invention of the instant application are not believed to be taught by Fang, applicant believes that claim 1 is allowable.

Issues 2-4 are not argued as claims 2-10 stand or fall with claim 1.

The honorable Board is therefore respectfully urged to reverse the final rejection of the Primary Examiner.

Respectfully submitted,

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Appendix - Appealed Claims:

1. A method for fabricating embedded nonvolatile semiconductor memory cells, which comprises the steps of:

providing a substrate divided into a high-voltage region, a memory region and a logic region;

forming a first insulating layer on the substrate in the high-voltage region, the memory region and the logic region;

removing the first insulating layer in the memory region;

forming a second insulating layer in the high-voltage region, the memory region and the logic region;

forming a charge storing layer in the high-voltage region, the memory region and the logic region;

patterning the charge-storing layer in the memory region;

forming a third insulating layer in the high-voltage region, the memory region and the logic region;

removing the first to third insulating layers and also the charge-storing layer in the logic region;

forming a fourth insulating layer in the high-voltage region, the memory region and the logic region; and

forming and patterning a conductive control layer in the high-voltage region, the memory region and the logic region.

2. The method according to claim 1, which comprises forming the first insulating layer by depositing an oxide layer having a thickness of 20 to 25 nm.

3. The method according to claim 1, which comprises thermally forming the second insulating layer as a tunnel oxide layer having a thickness of approximately 7 to 10 nm.

4. The method according to claim 1, which comprises forming a high-voltage oxide layer from the first and second insulating layers.

5. The method according to claim 1, which comprises forming the charge-storing layer as one of an electrically conductive layer and a nonconductive layer.

6. The method according to claim 1, which comprises forming the third insulating layer as an oxide-nitride-oxide layer sequence.

7. The method according to claim 1, which comprises during the second removing step, carrying out a dry etching step for removing the third insulating layer and the charge-storing layer.

8. The method according to claim 1, which comprises during the second removing step, carrying out a wet-chemical etching for removing the first and second insulating layers.

9. The method according to claim 1, which comprises forming the fourth insulating layer as a gate oxide layer by one of depositing the gate oxide layer and thermally forming the gate oxide layer.

10. The method according to claim 1, which comprises using a hard mask during the steps of forming and patterning the conductive control layer.